In the Specification

Paragraph beginning at page 3, line 20 has been amended as follows:

Figure 3 shows another prior art implementation (US PAT 5.260.610). This type of crossbar also needs (n / 2) x m memory elements **301** plus m memory elements **302**. To connect input line **303a** to output line **304** we must program a 1 in memory element **301** and a 1 in memory element **302**. But, by programming a one in memory element **301**, input line **303b** is connected to capacitance **306**. Capacitance **306** is large because it represents the parasitic load of half of the pass transistor of one column plus the metal interconnection between them. If the crossbar has 32 inputs, then capacitance **306** includes the parasitic load of 16 n-mos drains/sources. Again, the capacitive loading of one input line can vary dramatically with the programming pattern of the other inputs.

Paragraph beginning at page 4, line 4 has been amended as follows:

In applications where a significant number of crossbars are employed and interconnected, such as reconfigurable circuit applications, the input capacitive load variation of one crossbar input with respect to the programming pattern of its other inputs makes the timing optimization of high performance devices very difficult. Additionally, these and other prior art crossbar devices are found to consume more power and/or area than desired, as well as contributing to current swing.

Paragraph beginning at page 5, line 16 has been amended as follows:

In accordance with another aspect, a low power application of multiple crossbar devices to a reconfigurable circuit block is improved by having each memory element of a crossbar device be provided with a supply voltage higher by a threshold voltage Vth to maintain the supply voltage of corresponding output buffers input at Vdd, to prevent the output buffers from consuming static current when their inputs are at a degenerated level, to facilitate the lower power application.

Paragraph beginning at page 9, line 8 has been amended as follows:

As alluded to earlier, employing crossbar devices in a low power manner is especially desirable for an integrated circuit or integrated circuit block where a significant number of crossbar devices are employed and interconnected. An example of such integrated circuit is the scalable reconfigurable circuit disclosed in co-pending U.S. Patent Application, number 09/971,349, entitled "A Reconfigurable Integrated Circuit Having a Scalable Architecture", filed 10/4/2001, having common inventorship with present application. The specification of which is hereby fully incorporated by reference.

Paragraph beginning at page 9, line 20 has been amended as follows:

Figure 7 shows an improved crossbar output buffer structure to avoid static current at power-up, in accordance with yet another aspect of the present invention. As mentioned above, at power-up, the state of the memory elements are undefined.

This may create various paths between the inputs of a crossbar. For a reconfigurable circuit block, such as the one disclosed in co-pending application '349, many output buffers may be shorted together at power-up, producing a large current flow through the device. Also, during configuration loading sequence of the circuit block, the incomplete configuration may create temporary short circuits between the crossbar inputs. To compensate for these possibilities, the output buffers **704** are advantageously connected to a global control line **701** forcing their outputs to a known level. This control line is activated by a power-on reset circuitry **702** and is deactivated when a configuration has been loaded in the reconfigurable circuit block. Since all the crossbar outputs are at the same level during the power-up and until a configuration is loaded, the fact that they may or may not be shorted together does not produce any more current. For example, at power up, power on reset circuitry **702** resets the flip-flop **703**. The flip-flop output **701** forces all the crossbar buffers **704** to zero. When a configuration is loaded, flip flop **702** is written with a logical 1, enabling all crossbar output buffers.

In the Claims

Please amend the claims as follows:

1. (Once Amended) A crossbar device comprising:

n input lines;

m output lines; and

a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to selectively couple said n input lines to said m output lines;